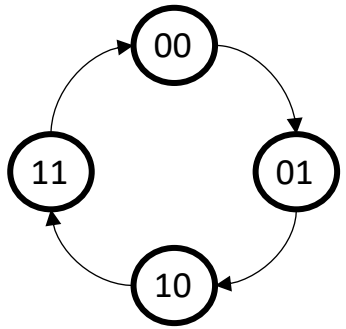
Asynchronous Counters

1. Not simultaneously counter.
2. Also Known as Ripple Counter.
3. CLK input for 1st Flip Flop are from external clock.
4. CLK input for next Flip Flop are from previous Flip Flop output.
5. Counting sequentially only either ascending (Up Counters) or descending (Down Counters)

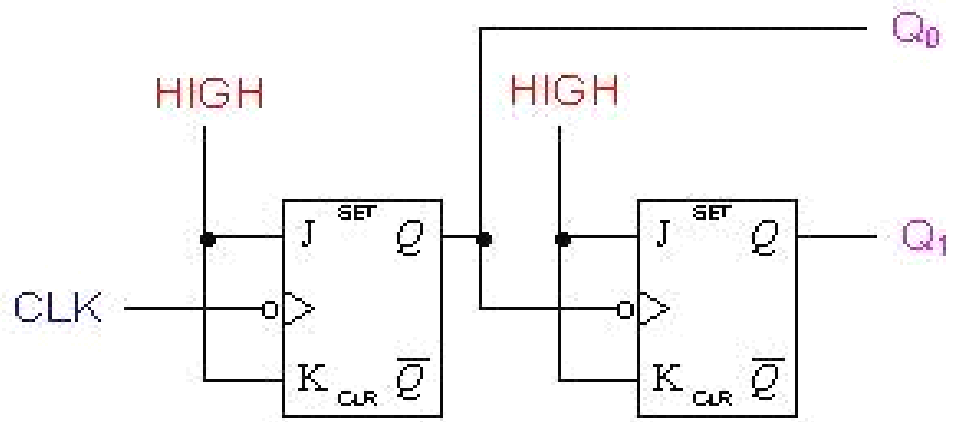
2-bit Asynchronous Up Counter (MOD 4)

Present State	Next State
Q_1Q_0	Q_1Q_0
00	01
01	10
10	11
11	00

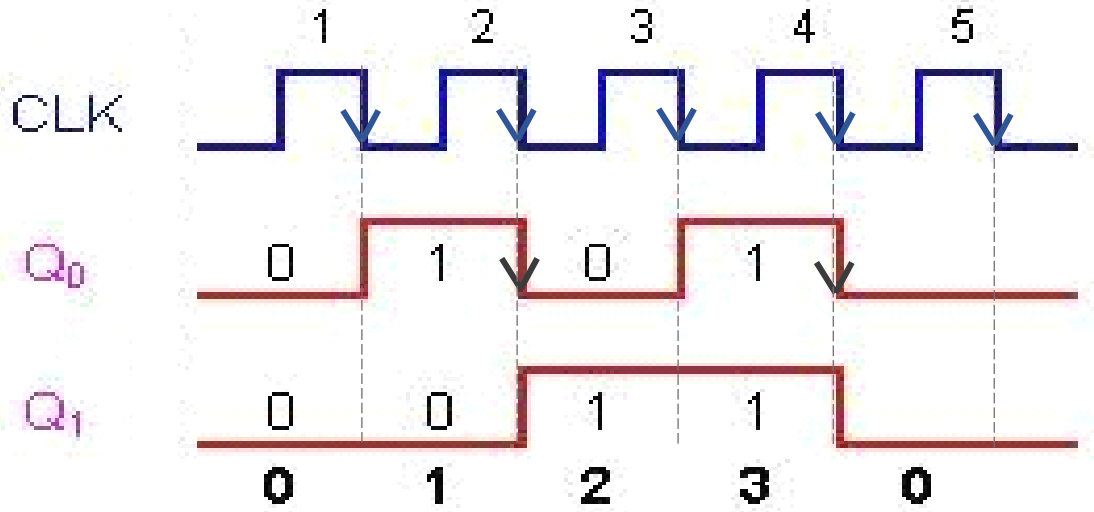
a. Next State Table



b. State Diagram



c. Circuit Diagram

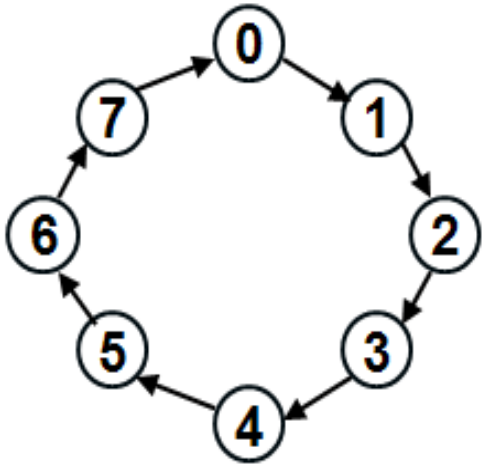


d. Timing Diagram

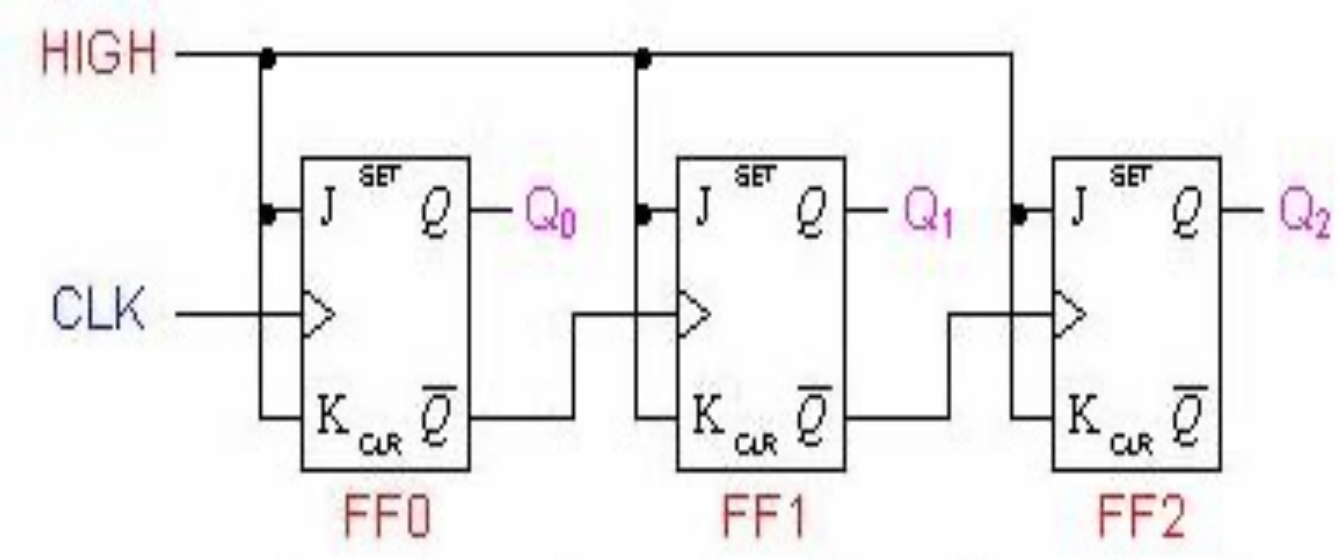
3-bit Asynchronous Up Counter (MOD 8)

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

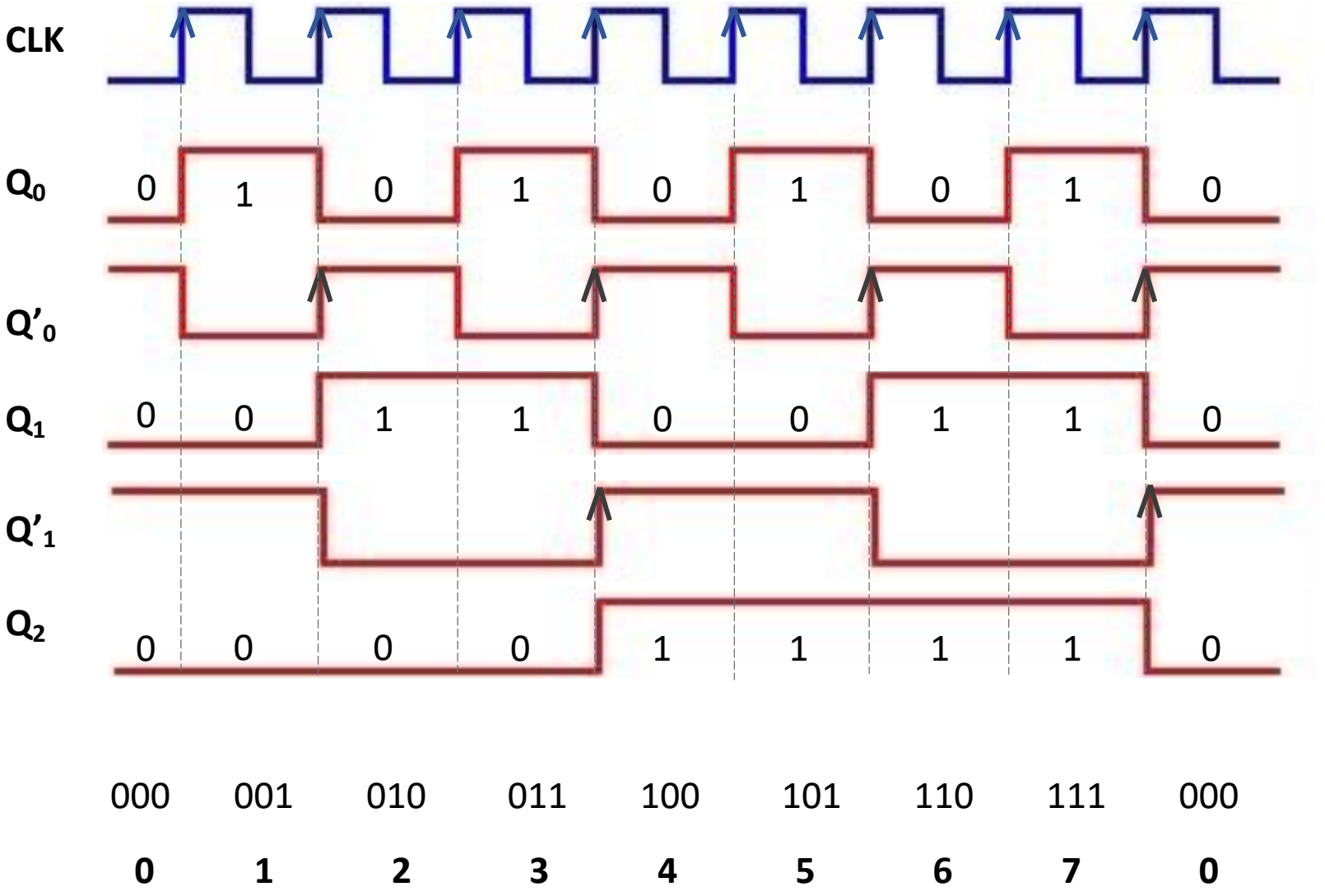
a. Next State Table



b. State Diagram

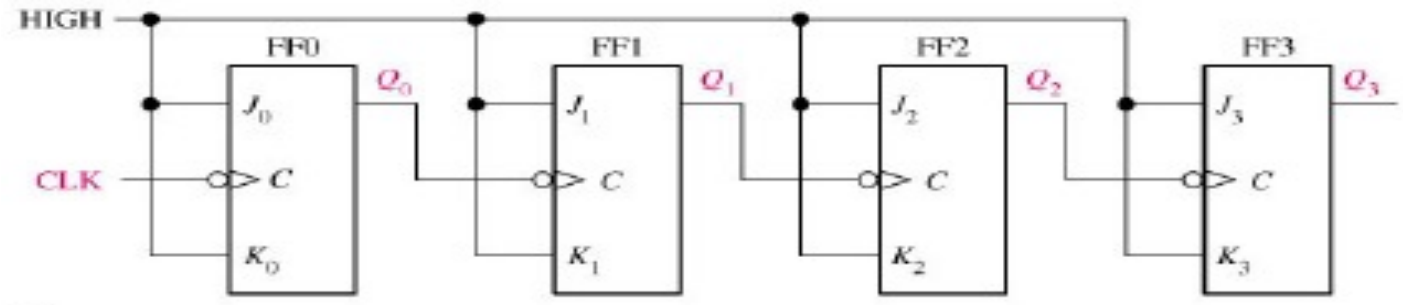


c. Circuit Diagram

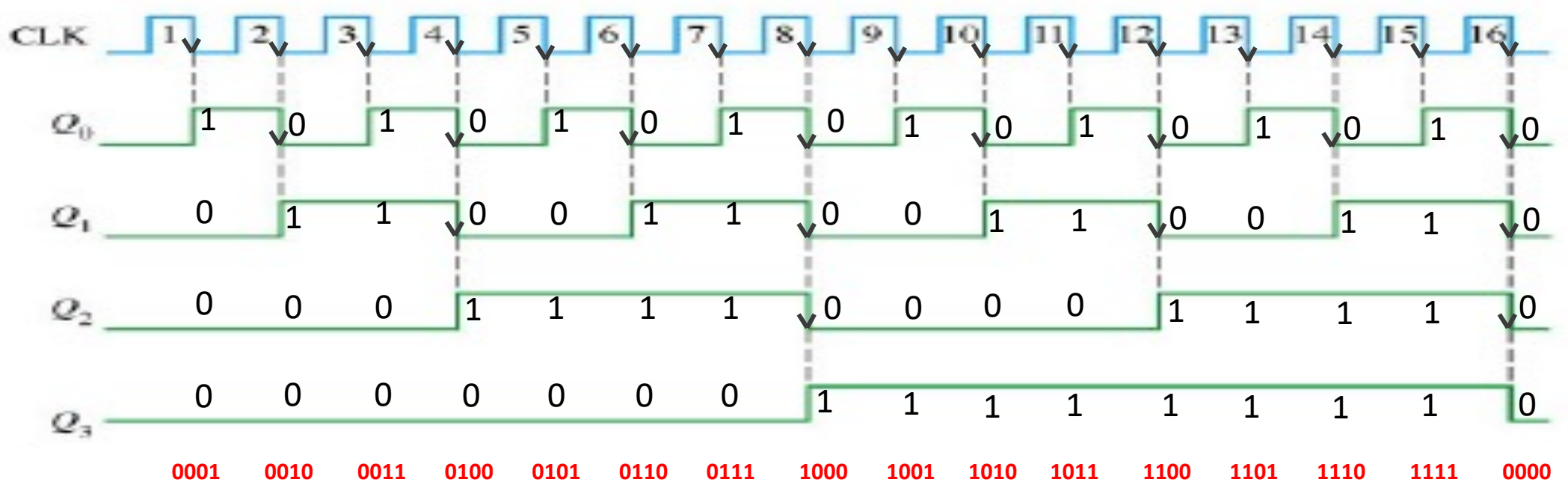


d. Timing Diagram

4-bit Asynchronous Up Counter (MOD 16)



a. Circuit Diagram

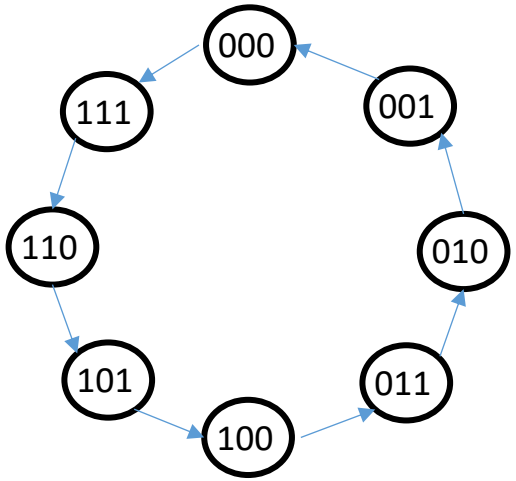


b. Timing Diagram

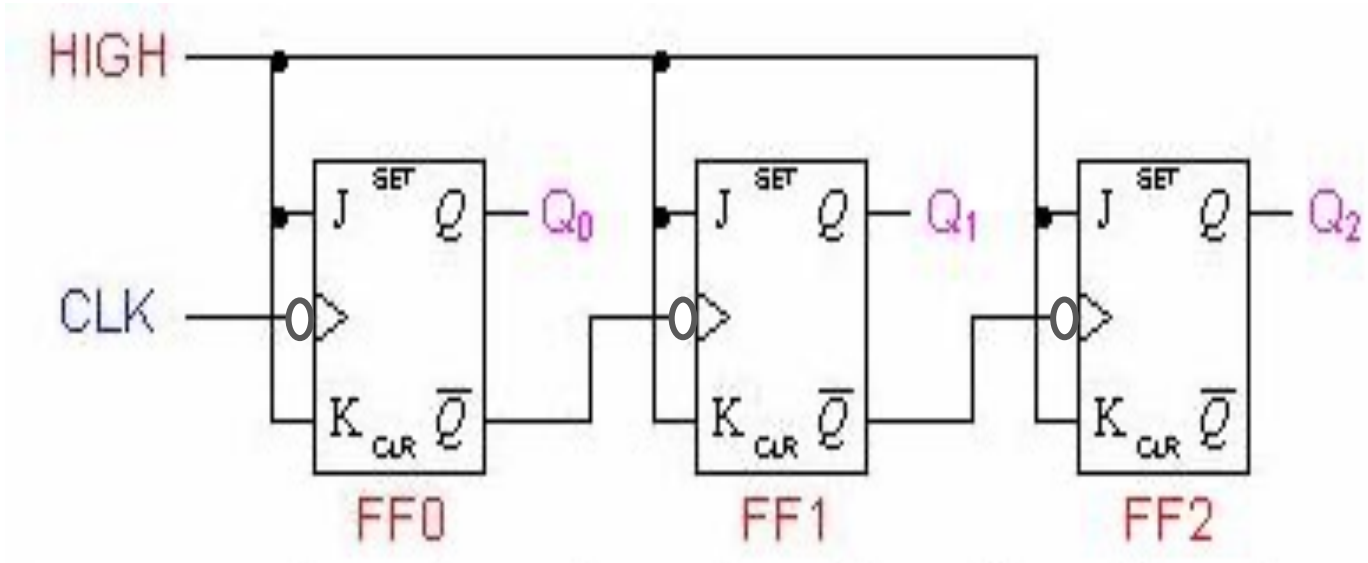
3-bit Asynchronous Down Counter (MOD 8)

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	1	1
1	1	1	1	1	0
1	1	0	1	0	1
1	0	1	1	0	0
1	0	0	0	1	1
0	1	1	0	1	0
0	1	0	0	0	1
0	0	1	0	0	0

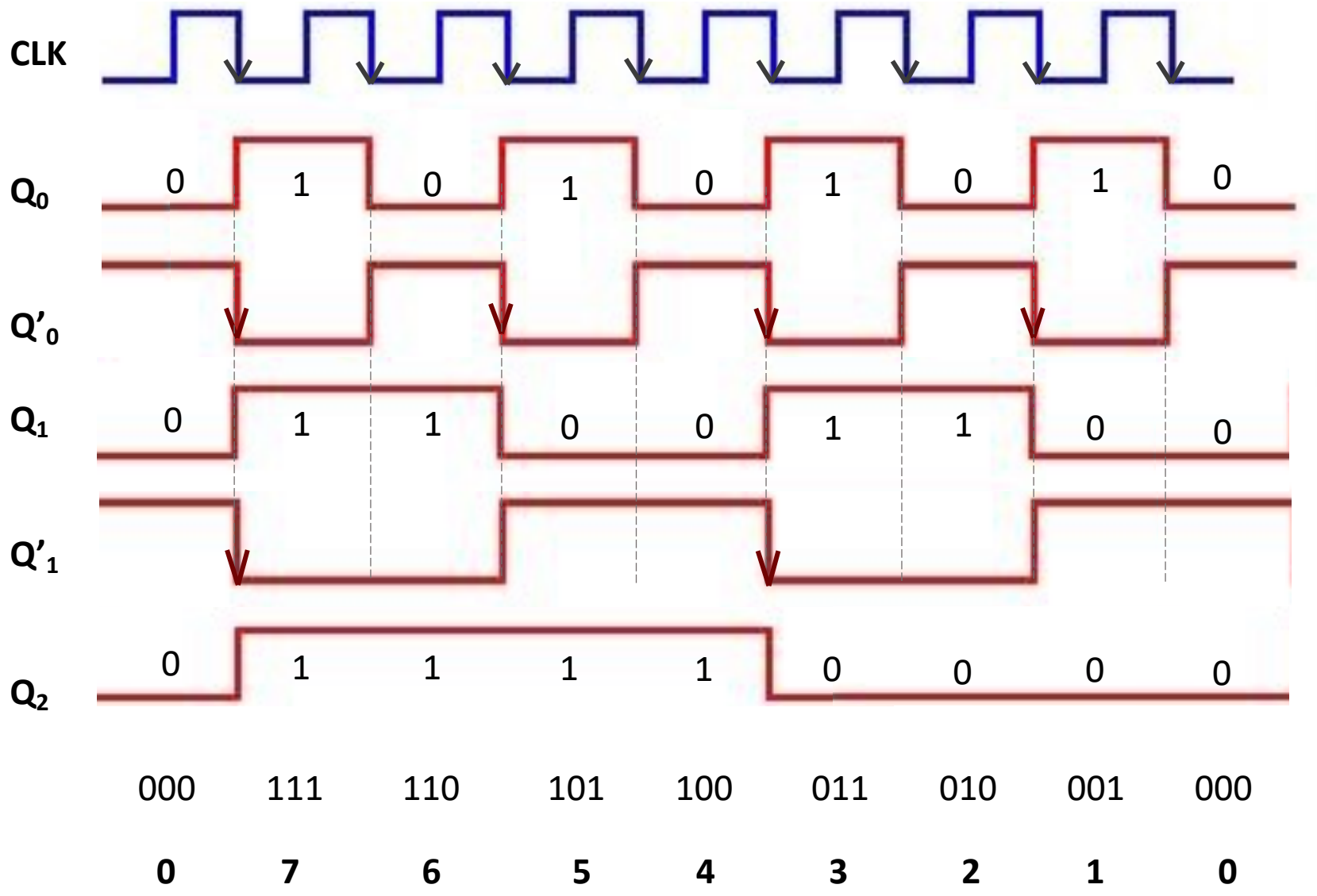
a. Next state table



b. State diagram



c. Circuit Diagram



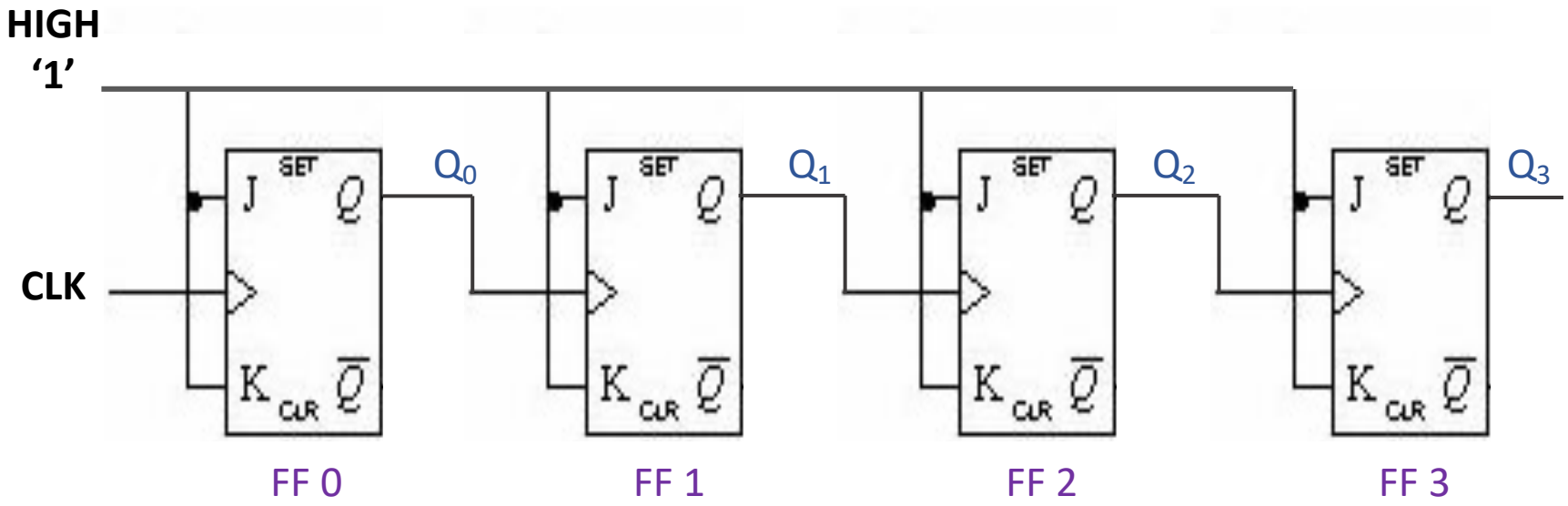
d. Timing Diagram

Asynchronous Counters Summary

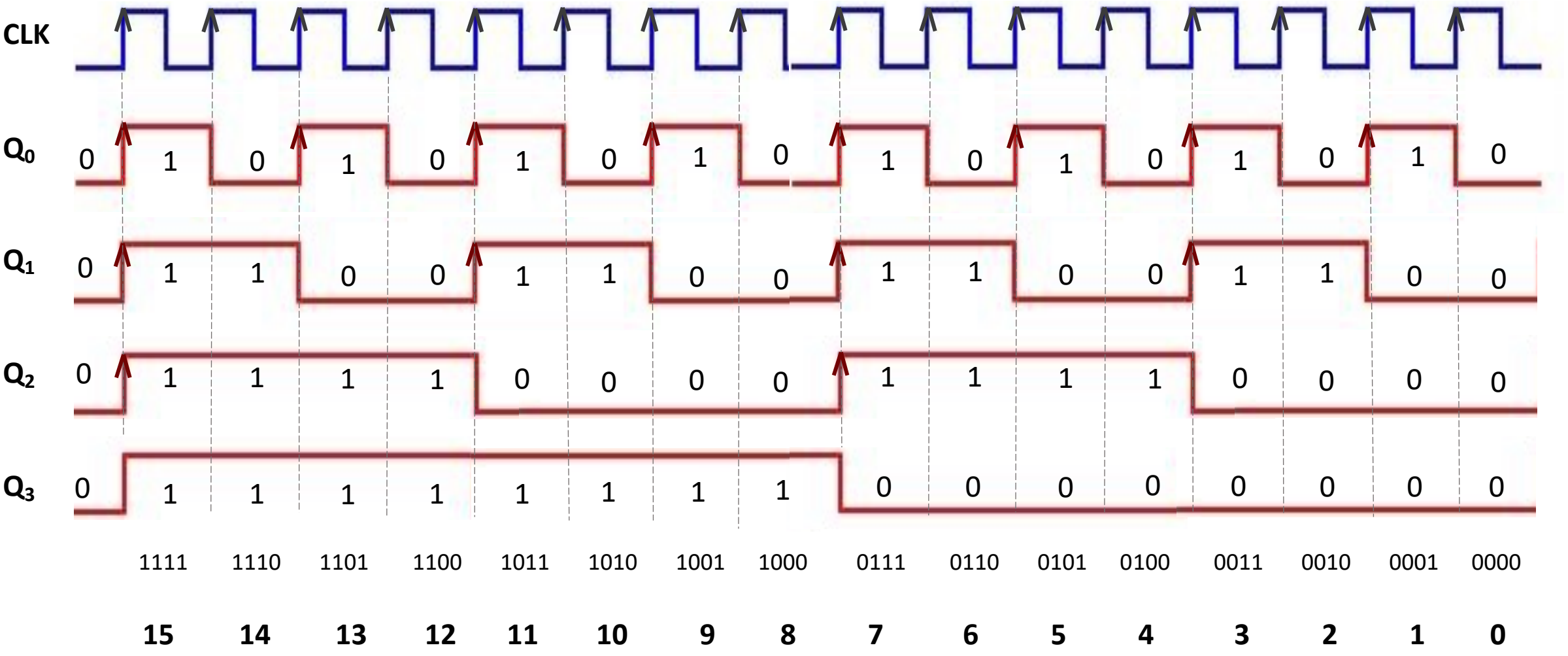
CLK JK FlipFlop	NEXT CLK (OUTPUT)	COUNTER
+VE (PGT)	$\overline{Q}$	UP
-VE (NGT)	Q	UP
+VE (PGT)	Q	DOWN
-VE (NGT)	$\overline{Q}$	DOWN

Exercise:

Draw Circuit Diagram and Timing Diagram for MOD 16 Asynchronous Down Counter using PGT Clock JK Flip Flop.



a. Circuit Diagram



b. Timing Diagram

Asynchronous Counter MOD Number $<2^n$

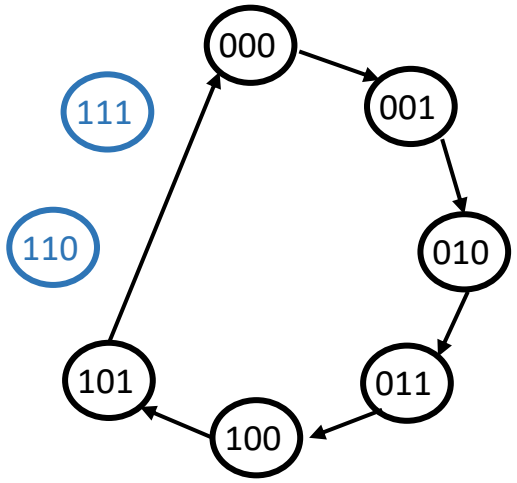
Example 1: MOD 6 Asynchronous Up Counter

Question:
How many Flip Flop needed?
From formula **$6 = 2^n$** How is **n**?

- This counter should count start from 0-1-2-3-4-5 only.
- Before reach 6, this counter should back to “0”
- Use appropriate gate to activate CLEAR function on each Flip Flop.

* When CLEAR get ‘1’ , counter circuit will reset to ‘0’

Present State			Next State		
Q_C	Q_B	Q_A	Q_C	Q_B	Q_A
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0



a. Next state table

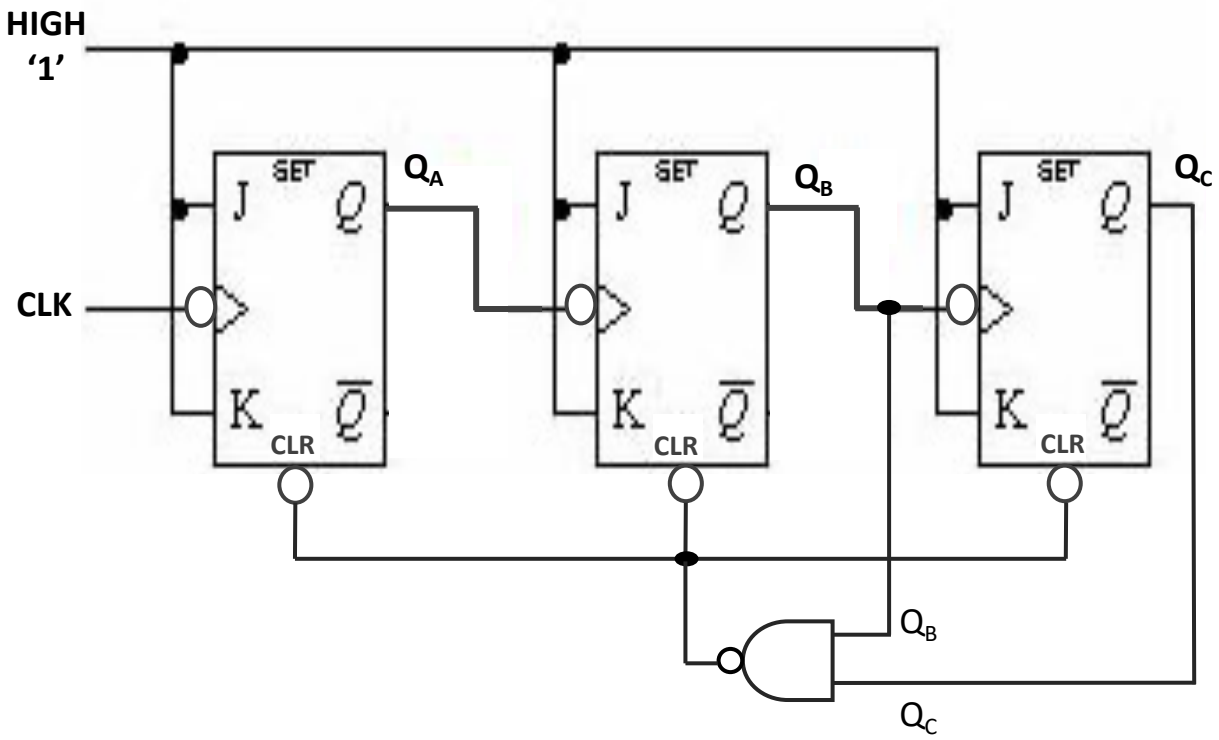
b. State diagram

Counting sequences:

Q_C	Q_B	Q_A	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	← Stop counting HERE!! Where **C=1** and **B=1**

Using NAND Gate:

Q_C	Q_B	OUT	
0	0	1	
0	1	1	
1	0	1	
1	**1**	**0**	← We need output '0' to make all CLR '1' and The Counter reset to zero.



c. Circuit Diagram

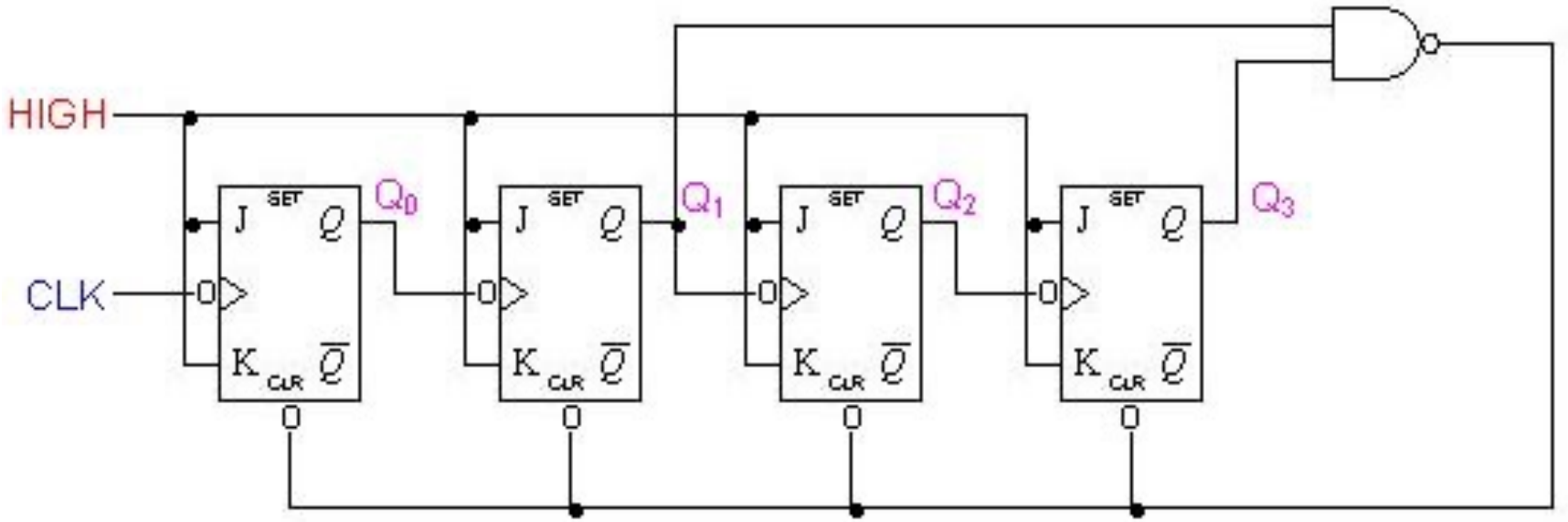
Example 2: Asynchronous Decade Counter (Mode 10)

- Once the counter counts to ten (1010), all the flip-flops are being cleared.
- Notice that only Q1 and Q3 are used to decode the count of ten.
- This is called partial decoding, as none of the other states (zero to nine) have both Q1 and Q3 HIGH at the same time.

Present State				Next State			
Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0

1 0 1 0 ← Stop counting HERE!!
Where **Q3=1** and **Q1=1**

Next state table



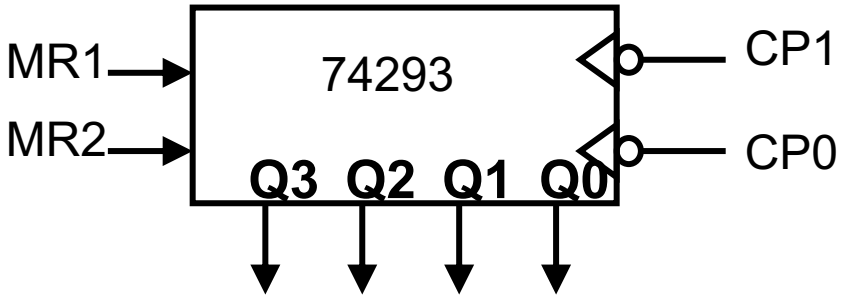
Circuit Diagram

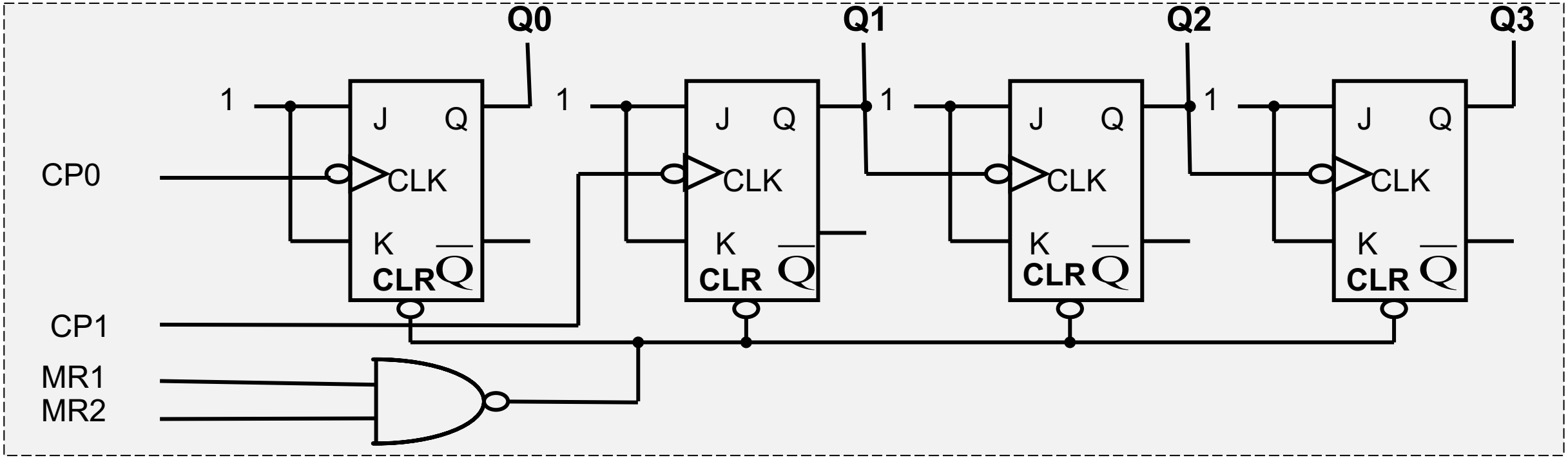
Exercise:

Design MOD 12 Asynchronous Up Counter. Draw the Circuit Diagram.

IC for Asynchronous counters (IC 74293)

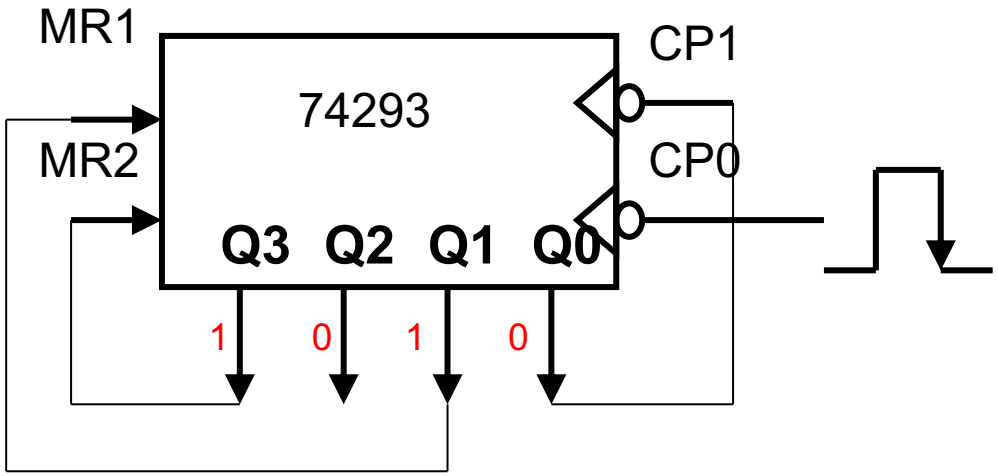
- 74293 IC for Asynchronous counter with Reset (MR1 and MR2)





IC for Asynchronous counters (IC 74293)

Example 1: Asynchronous Decade Counter (Mode 10)



Example 2: Asynchronous Counter Mode 14