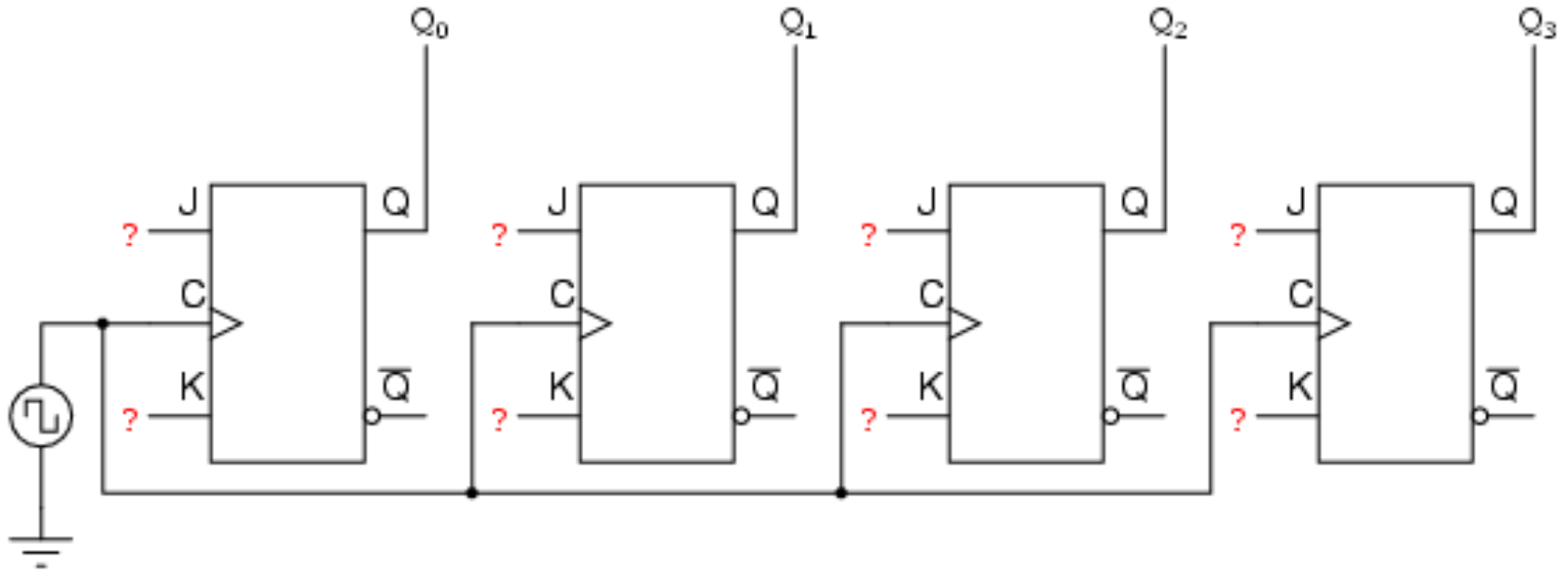
Synchronous Counters

- A *synchronous counter*, in contrast to an *asynchronous counter*, is one whose output bits change state simultaneously, with no ripple.
- The only way we can build such a counter circuit from J-K flip-flops is to connect all the clock inputs together, so that each and every flip-flop receives the exact same clock pulse at the exact same time:



Example: General Circuit Diagram

How To Design Synchronous Counters

- For synchronous counters, all the flip-flops are using the same CLOCK signal. Thus, the output would change synchronously.
- Procedure to design synchronous counter are as follows:-

  STEP 1: Obtain the State Diagram.

  STEP 2: Obtain the Excitation Table using state transition table for any particular FF (JK or D). Determine number of FF used.

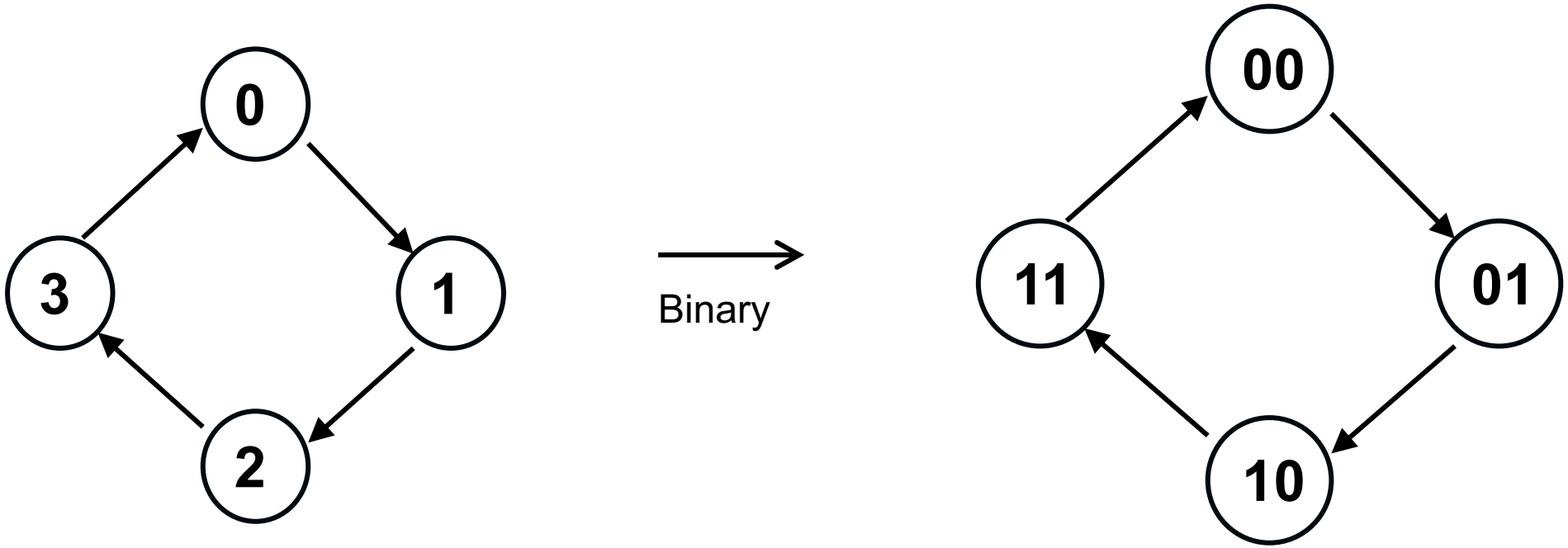
  STEP 3: Obtain and simplify the function of each FF input using K-Map.

  STEP 4: Draw the circuit.

Synchronous Counters

Example 1: Design a MOD-4 Synchronous Up Counter, using JK FF.

STEP 1: Obtain the State transition Diagram



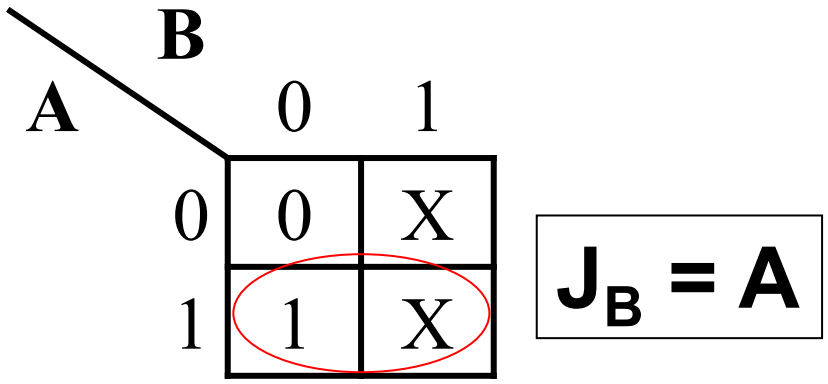
STEP 2: Obtain the Excitation table. Two JK FF are used.

OUTPUT TRANSITION			FF INPUT	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

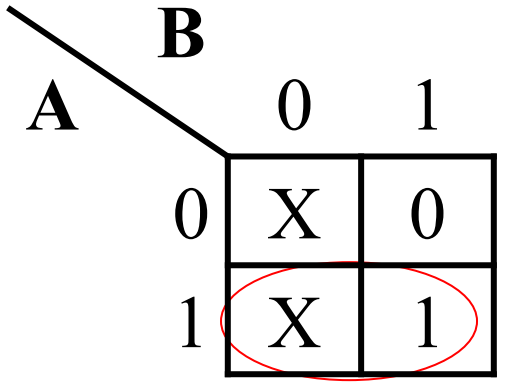
Excitation table

Present State		Next State		Input, J K			
B	A	B	A	J_B	K_B	J_A	K_A
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

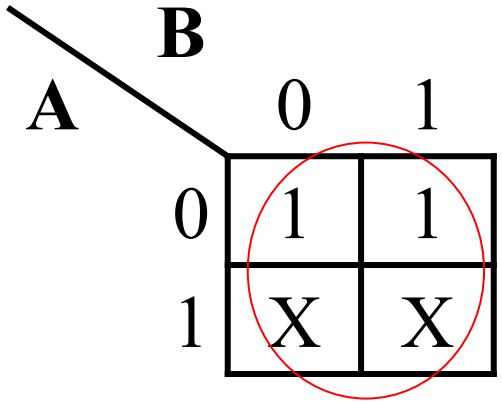
STEP 3: Obtain the simplified function using K-Map (Refer to input AB present state)



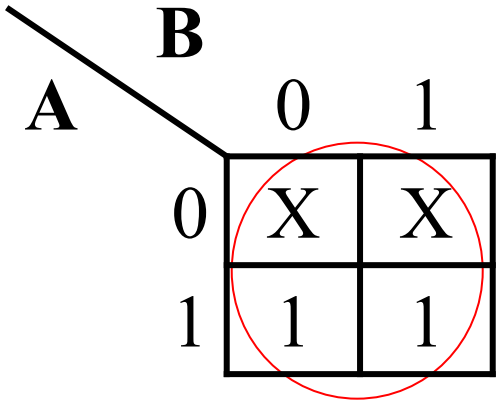
$J_B = A$



$K_B = A$



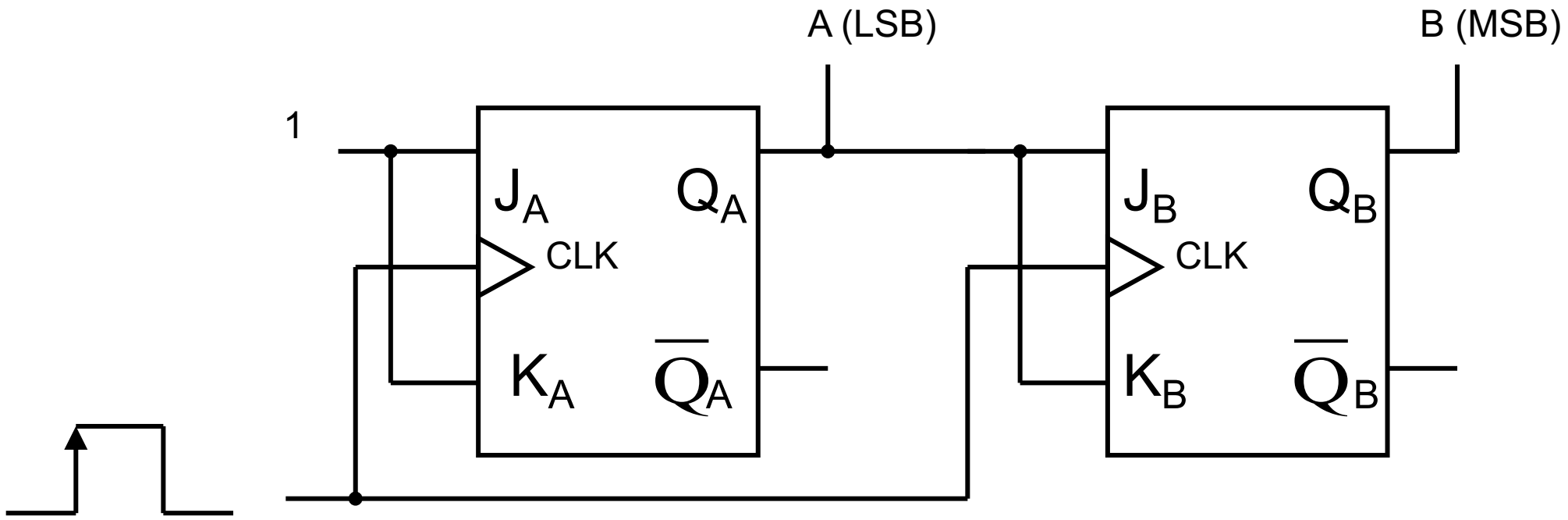
$J_A = 1$



$K_A = 1$

STEP 4: Draw the circuit diagram

$J_B = A$ $K_B = A$ $J_A = 1$ $K_A = 1$

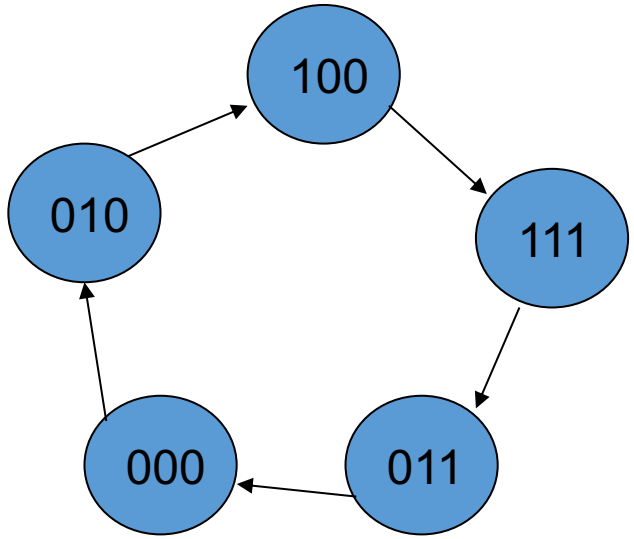


(MOD-4 Synchronous Up Counter)

Synchronous Counters

Example 2: Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JK Flip Flop negative triggered

STEP 1: Obtain the State transition Diagram



STEP 2: Obtain the Excitation table.

* Maximum Decimal Number is 7 = **1 1 1** in 3 bit binary, so 3 JK FF are used.

OUTPUT TRANSITION			FF INPUT	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Excitation table

Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
4	1	0	0	1	1	1	x	0	1	x	1	x
7	1	1	1	0	1	1	x	1	x	0	x	0
3	0	1	1	0	0	0	0	x	x	1	x	1
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x

K-Map For

$J_A = Q_C$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	0	0	X	1
A	X	X	X	X

K-Map For

$K_A = \overline{Q_C}$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	X	X	X	X
A	X	1	0	X

STEP 3: Obtain the simplified function using K-Map (Refer to input AB present state)

K-Map For

$J_B = 1$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	1 (4)	X (5)	X	1 (1)
A	X	X (3)	X (2)	X

K-Map For

$K_B = \overline{Q_C}$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	X	1	X	X
A	X	1	0	X

K-Map For

$$J_C = \overline{Q_A} \cdot Q_B$$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	0	1	X	X
A	X	0	X	X

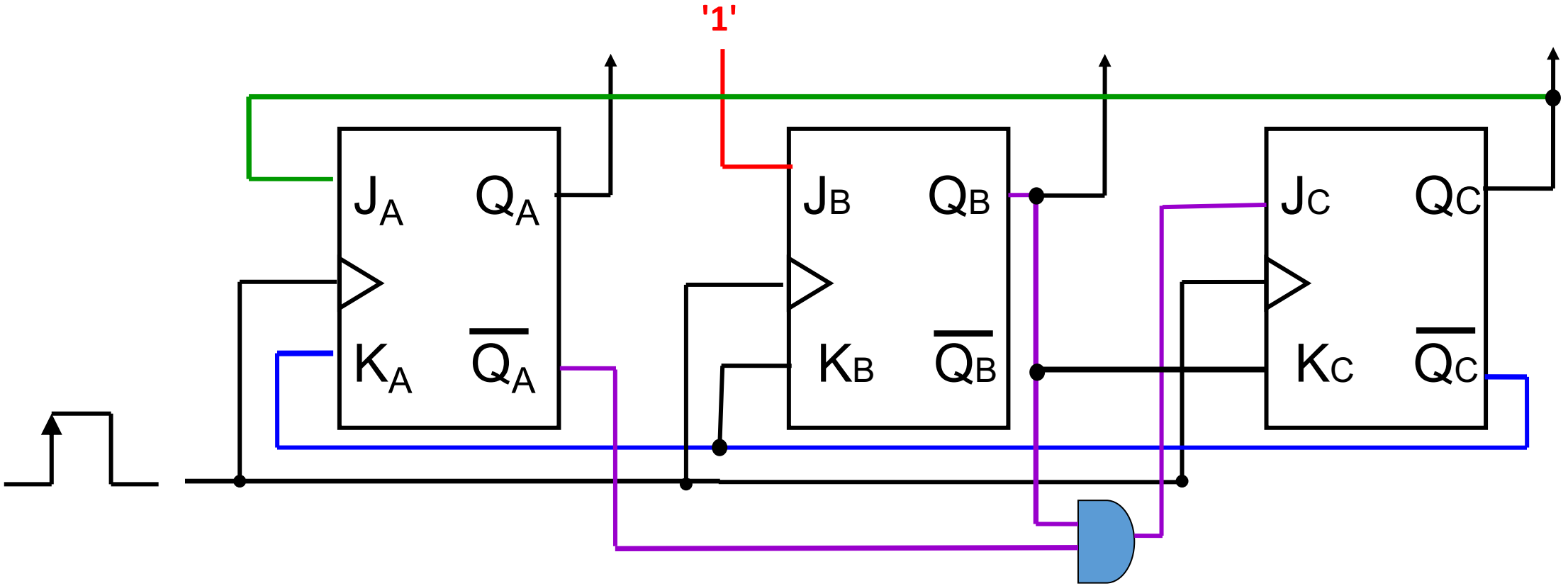
K-Map For

$$K_C = Q_B$$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	X	X	X	0
A	X	X	1	X

STEP 4: Draw the circuit diagram

$J_A = Q_C$ $K_A = \overline{Q_C}$ $J_B = 1$ $K_B = \overline{Q_C}$ $J_c = \overline{Q_A} \cdot Q_B$ $K_C = Q_B$



Exercise:

Design Counter to count the following sequence; 6 – 4 – 2 – 3 – 1
Draw the Circuit Diagram.

Example: Design synchronous counter that counting from 0-1-3-7

* Maximum Decimal Number is 7 = **1 1 1** in 3 bit binary, so 3 JK FF are used.

OUTPUT TRANSITION			FF INPUT	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Excitation table

Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	1	0	X	1	X	X	0
3	0	1	1	1	1	1	1	X	X	0	X	0
7	1	1	1	0	0	0	X	1	X	1	X	1

Obtain the simplified function using K-Map (Refer to input AB present state)

K-Map For

$J_A = 1$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	1 1	X	X	X
A	2 X	3 X	4 X	X

K-Map For

$K_A = Q_C$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	X	X	X	X
A	0	0	1	X

K-Map For

$J_B = Q_A$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	0	X	X	X
A	1	X	X	X

K-Map For

$K_B = Q_C$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	X	X	X	X
A	X	0	1	X

K-Map For

$J_C = Q_B$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	0	X	X	X
A	0	1	X	X

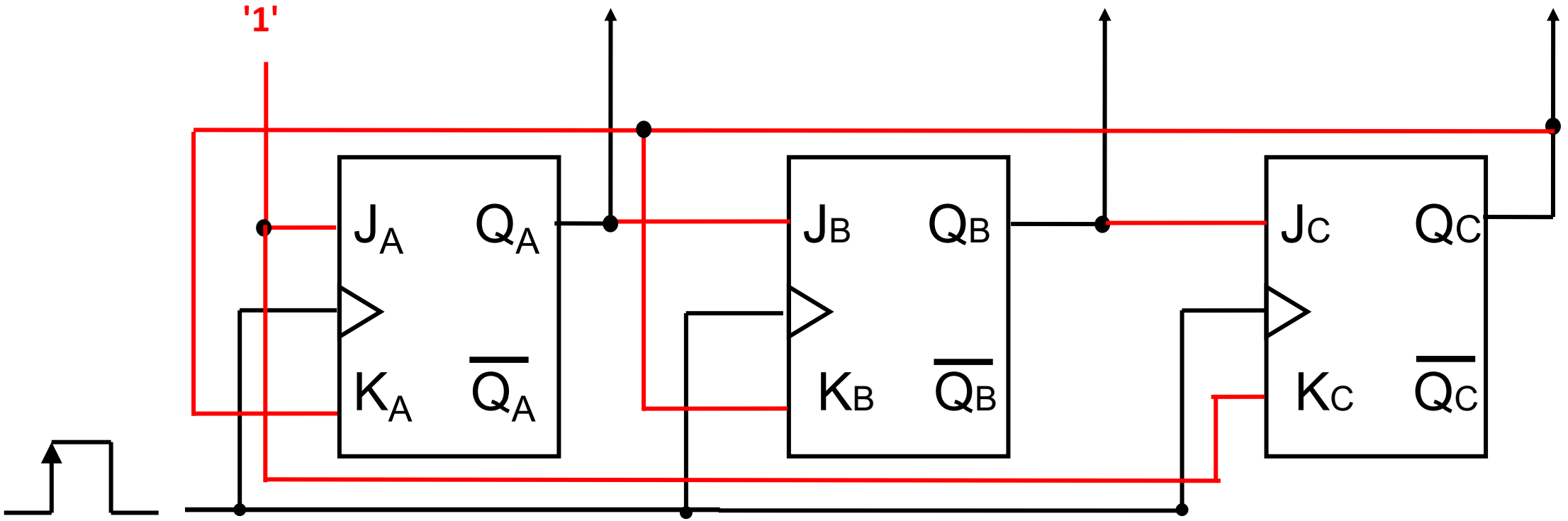
K-Map For

$K_C = 1$

	$\overline{C}\overline{B}$	$\overline{C}B$	CB	$C\overline{B}$
$\overline{A}$	X	X	X	X
A	X	X	1	X

Draw the circuit diagram

$J_A = 1$ $K_A = Q_C$ $J_B = Q_A$ $K_B = Q_C$ $J_c = Q_B$ $K_C = 1$



Example: Design synchronous counter that counting from 0-1-3-4-5-7 using T Flip Flop

* Maximum Decimal Number is 7 = **1 1 1** in 3 bit binary, so 3 T Flip Flop are used.

OUTPUT TRANSITION Q_N → Q_{N+1}	FF INPUT T
0 → 0	0
0 → 1	1
1 → 0	1
1 → 1	0

Excitation table for T Flip Flop

Decimal	Present State			Next State			T_C	T_B	T_A
	Q_C	Q_B	Q_A	Q_C	Q_B	Q_A			
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	1	0	1	0
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	1	0	1	0
7	1	1	1	0	0	0	1	1	1

Obtain the simplified function using K-Map (Refer to input AB present state)

K-Map For

$T_C = B = Q_B$

	$\overline{B}\overline{A}$	$\overline{B}A$	BA	$B\overline{A}$
$\overline{C}$	0	0	1	X
C	0	0	1	X

K-Map For

$T_B = A = Q_A$

	$\overline{B}\overline{A}$	$\overline{B}A$	BA	$B\overline{A}$
$\overline{C}$	0	1	1	X
C	0	1	1	X

K-Map For

$T_A = \overline{B} = \overline{Q_B}$

	$\overline{B}\overline{A}$	$\overline{B}A$	BA	$B\overline{A}$
$\overline{C}$	1	1	0	X
C	1	1	0	X

Draw the circuit diagram

$T_C = Q_B$, $T_B = Q_A$, $T_A = \overline{Q_B}$